Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
V SEMESTER BACK-PAPER EXAMINATION- 2005

LEVEL : B. E. (Computer)
SUBJECT: BEG372CO, Computer Organization & Design.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
The marks allotted for each sub-question is specified along its side.
Attempt ALL questions.

Q. [1] What is computer organization and computer design? Explain the layered view of a computer system. [2+6]

Q. [2] What is gate array? How is it advantageous than other chips? Write the HDL for fetch cycle of CPU. [2+3+3]

Q. [3] **[a]** Explain floating point binary number representation technique. Normalize the number ($.00101100\times10^{10}$). [4+2]
[b] A 12-bit wo4d red form memory has 8-data bits (10001011) and 4-check bits (0110). Determine the error bit position if the word has error. [6]

Q. [4] **[a]** Explain Phase, Decode and Execution cycle of an instruction execution. Differentiate between RISC and CISC machine. [4+4]s
[b] Divide 12 (1100) by 5 (0101) showing the steps using restoring division method. [6]

Q. [5] What is bit-sliced ALU? Explain arithmetic processor as coprocessor. Describe different sources of interrupt. [2+4+4]

Q. [6] What are the differences between hardwired and Microprogrammed control unit? Explain sequence counter method of hardwired control design. [2+4]

Q. [7] **[a]** Explain the RZ (returned to zero) and NRZI (non-return to zero inverted) digital recording schemes. [2+2]
[b] In a CRC logic, k-bit message Mi can be converted into n-bit encoded message by appending (n-k) check bits. So that x^{n-k}. $M_i = G(x). Q(x)+R(x)$ where G(x), Q(x) and R(x) are divisor, quotient and remainder polynomial. If M_i = 1101, n = 7 and $G(x) = x^2+x+1$, what will be the encoded message? [6]

Q. [8] Explain the architecture of memory subsystem. [6]

Q. [9] **Write short notes on (any TWO): [3+3=6]**
[a] Complexity of computing.
[b] Virtual Memory.
[c] Semantic Gap.
[d] IO Channel/ Processor.

Downloaded from www.jayaram.com.np

Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
V SEMESTER FINAL EXAMINATION- 2005

LEVEL : B. E. (Computer)
SUBJECT: BEG372CO, Computer Organization & Design.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
The marks allotted for each sub-question is specified along its side.
Attempt ALL questions.

Q. [1] On what basis ban parallel processing be classified. Briefly describe four major groups of classification of parallel processing. [1+5]
Q. [2] What is Fetch-decode-execute cycle? Explain it in steps. [4]
Q. [3] Describe briefly the different modes of data transfer techniques. [6]
Q. [4] How are errors detected in data transmission? Explain with the help of parity generator and checker circuit. [5]
Q. [5] What is complexity of computing ? Describe briefly the three models of computing. [2+6]
Q. [6] What is control unit? Explain the implementation of control unit for programmable system and for a non-programmable system. [8]
Q. [7] Briefly describe the architecture of memory subsystem. [4]
Q. [8] What are semiconductor memories? Explain in brief about Gap filler memories. [2+3]
Q. [9] The transfer rate between CPU and its associated memory is orders of magnitude higher than the mechanical I/O transfer rate. How can this imbalance cause inefficiencies? How can it be alleviated? [5]
Q. [10] Explain any one of the digital recording methods with necessary diagrams. [4]
Q. [11] Explain about the Input Output Interrupt. Explain the process of input output transfer. [4+3]
Q. [12] What are the necessary conditions for interfacing CMOS and TTL. Draw the voltage and current level of CMOS –to-TTL and TTL-to CMOS interfacing. [2+6]
Q. [13] Write short notes on (any TWO) [5+5=10]
[a] Virtual Memory.
[b] Semantic Gap
[c] ISA

Downloaded from www.jayaram.com.np

Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
V SEMESTER FINAL EXAMINATION- 2006

LEVEL : B. E. (Computer)
SUBJECT: BEG372CO, Computer Organization & Design.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
The marks allotted for each sub-question is specified along its side.
Attempt ALL questions.

Q. [1] **[a]** Write the difference layers of computer system and explain their interfacing? [5]
[b] State the difference between manual and machine computation. [5]

Q. [2] **[a]** Define HDL? What are the different types of RTL components , state with example. [2+4]
[b] Explain the basic concept of TTL to CMOS interfacing. [4]

Q. [3] **[a]** Mention the types of generic operations that can be performed on data. Briefly describe how the logical instructions are executed. [2+8]

Q. [4] **[a]** Write Booth's multiplication algorithm. Using this algorithm calculate the value of 11X5. [5+5]

Q. [5] **[a]** Develop error correction code for 16 bit word. Generate the code for 1101000000110001.How many checks bits are required to detect single bit error in 512 hardwired control unit. [4+4+2]

Q. [6] **[a]** Describe the microprogammed control unit. State the difference between microprogrammed control unit and hardwired control unit. [8+2]

Q. [7] **[a]** What do you mean by the impact of memory sped on CPU's processing power. How this problem can be overcome. [3+3]
[b] Define Virtual memory and Flash Memory. [2+2]

Q. [8] **[a]** Explain ISA By giving proper illustration describe how parallel processing enhances the performance. [4+6]

Q. [9] **Write short notes on (any TWO): [5+5=10]**
[a] Self defining data types.
[b] Gate arrays.
[c] Memory Hierarchy.
[d] Control Unit.

Downloaded from www.jayaram.com.np

Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
V SEMESTER FINAL EXAMINATION- 2006

LEVEL : B. E. (Computer)
SUBJECT: BEG372CO, Computer Organization & Design.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
The marks allotted for each sub-question is specified along its side.
Attempt ALL questions.

Q. [1] **[a]** Explain the layered view of a computer system with its system architecture. [10]

Q. [2] **[a]** Suppose an 8-bit data word stored in memory is 11011100. Using the hamming algorithm determine the check bits stored. [8]
[b] Suppose the checks bits stored in memory is 1101 and the check bits recalculated from the 8-bit data word read from memory is 1000. Is there any error in 8-bit data word? If yes, then which bit needs to be changed? Calculate. [2]

Q. [3] **[a]** Define semiconductor memory. Explain the working of DRAM with a neat diagram. [5]
[b] What is an Arithmetic Processor? Explain arithmetic processor as coprocessor. [5]

Q. [4] **[a]** Describe the hardwired implementation of Control Unit with neat diagram. [5]
[b] What are different methods of fixed point representation? Explain. [5]

Q. [5] **[a]** What is semantic gap? Explain the problems caused by semantic gap?. [5]
[b] Find the product of 01011 and 00101 using Booth's Multiplication algorithm. (Show steps). [8]

Q. [6] **[a]** What is Multiple Module Memory? What is the importance of Virtual Memory? [5]
[b] How data are written into and read form magnetic tape? [5]

Q. [7] **[a]** Describe the architecture of memory subsysm alogn with its hierarchy. [5]
[b] What are the importance of computer graphics? [2]

Q. [8] **Write short notes on (any TWO): [5+5=10]**
[a] Complexity of Computing.
[b] Interrupt Cycle.
[c] Gate array.

Downloaded from www.jayaram.com.np

Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
V SEMESTER FINAL EXAMINATION- 2007

LEVEL : B. E. (Computer)
SUBJECT: BEG372CO, Computer Organization & Design.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
The marks allotted for each sub-question is specified along its side.
Attempt ALL questions.

Q. [1] **[a]** Compare between 'Difference engine' and analytical engine' developed by Charles Babbage. [3]
[b] What are the areas to which the discipline of computer science and engineering deals? [3]

Q. [2] **[a]** perform $(4)_{10}/(2)_{10}$ [5]
[b] How will you know that the driving gate is capable to drive the driven gate? [3]

Q. [3] What is syndrome world in any error correction method? Explain how it is interpreted for hamming code method with its characteristics. [2+2+2]

Q. [4] **[a]** What is instruction cycle? Describe fetch cycle with the suitable timing diagram. [2+4]
[b] Differentiate between the arithmetic processor as coprocessor and auxiliary processor. [3]

Q. [5] **[a]** What is interrupt cycle? [3]
[b] Explain control word and control memory with respect to micro programmed control unit. [3+3]

Q. [6] **[a]** Explain how a stored data is read from associative memory. [4]
[b] What is demand paging ? State the purpose translation look aside buffer (TLB) used in virtual memory. [3+3]

Q. [7] Explain about the return to zero (RZ) digital recording methods with necessary example. [5]

Q. [8] What is DMA (Direct Memory Access)? Explain its working principle. [2+6]

Q. [9] **[a]** Explain how performance and cost are related with each other for the evaluation of any computer architecture. [4]
[b] Describe in brief about the architecture of memory subsystem. [5]

Q. [10] **Write short notes on (any TWO): [5+5=10]**
[a] Gate array.
[b] Shift micro operation.
[c] Printers.

Downloaded from www.jayaram.com.np

Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
V SEMESTER BACK-PAPER EXAMINATION- 2004

LEVEL : B. E. (Computer)
SUBJECT: BEG372CO, Computer Organization & Design.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-questions is specified along its side. .
Attempt ALL questions.

Q. [1] **[a]** Explain the different layers of computer system along with their interface. [8]
[b] What are electromechanical machines? [2]

Q. [2] **[a]** How do you interface CMOS to TTL? Explain CAD tools. **[4+4]**
[b] How do you represent a fixed point binary number? [2]

Q. [3] **[a]** Draw a 4×4 stack using shift register cells as building blocks and explain is working. [8]
[b] What is cache memory? [2]

Q. [4] **[a]** Explain hardwired implementation of control unit. [5]
[b] Explain the working of DRAM with neat diagram. [5]

Q. [5] **[a]** Write an algorithm for fixed point multiplication with an example. [5]
[b] Explain the working of magnetic medium and magnetic head. [5]

Q. [6] **[a]** What do you mean by synchronous and asynchronous modes of data transfer?
[b] Explain instruction pipelining.

Q. [7] **[a]** For the 8-bit work 00111001, the check bits store with it would be 0111 . Suppose when the word read from memory, the check bits are calculated be 1101. What is the data word that was read from the memory ? [8]
[b] Give different stages of an instruction cycle. [2]

Q. [8] **Write short notes on :** **[5+5]**
[a] Multiple Module Memory.
[b] Arithmetic Processors.

Downloaded from www.jayaram.com.np

Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
2008
B. E. (Computer)/Fifth Semester/Final
Time 03:00 hrs. Full Marks: 80/Pass Marks: 32

BEG372CO, Computer Organization & Design.

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-question is specified along its side.
Answer EIGHT questions.

Q. [1] Explain different layer of computer system and their interface. Explain different sequential RTL components. [5+5]

Q. [2] How are the floating point and fixed point data represented in computer system? Write down how addition and subtraction is performed when numbers are represented in 1's complement form. [5+5]

Q. [3] **[a]** Discuss different groups of machine instructions. [5]
[b] What is interrupt cycle? Explain the various sources of interrupt. [2+3]

Q. [4] How is any instruction executed by CPU? Differentiate hardwired and microprogammed control unit. [4+6]

Q. [5] **[a]** What are the storage technologies? [3]
[b] Explain Gap filler memory. How does it overcomes the problem of cost an performance regarding other memory system. [4+3]

Q. [6] Explain the need of secondary storage in computer system. How is information stored in magnetic and optical devices? **[3+7]**

Q. [7] **[a]** What are the different transfer techniques? [4]
[b] Explain the various types of Video Display Unit (VDU). [6]

Q. [8] Why do we need parallel processing mechanism? Explain SIMD and MIMD model of computation. [3+7]

Q. [9] Write short notes on any TWO: [2×5=10]
[a] I/O Interrupts **[b]** RISC **[C]** Virtual memory.

Downloaded from www.jayaram.com.np

Downloaded from www.jayaram.com.np

PURWANCHAL UNIVERSITY
2009
B. E. (Computer)/Fifth Semester/Final
Time 03:00 hrs. Full Marks: 80/Pass Marks: 32

BEG372CO, Computer Organization & Design.

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-question is specified along its side.
Answer EIGHT questions.

Q. [1] **[a]** Describe the computer system design according to structural and layout point of view. [4]
[b] What is complexity of computing? Explain any two models of computing. [2+4]

Q. [2] **[a]** How can you develop the interfacing circuit form CMOS to TTL and TTL to CMOS? [5]
[b] What are the basic features of HDL? [5]

Q. [3] **[a]** Explain sign magnitude, 1'a complement and 2's complement format of fixed point representation? What are the various built-in-data types? [3+2]
[b] Define the term 'Semantic gap'? Specify its net impact. **[1+4]**

Q. [4] **[a]** Explain Arithmetic processor as a coprocessor. [5]
[b] Compare RISC and CISC architecture. [5]

Q. [5] **[a]** What is fetch cycle and execution cycle? [4]
[b] Describe micro-programmed control unit with its various steps to execute microinstruction. [6]

Q. [6] **[a]** What is the solution for speed mismatch between main storage and CPU? [4]
[b] Describe Associative memory and gap filler memory in brief. [6]

Q. [7] **[a]** Explain RZ and NRZ digital recording scheme. [5]
[b] How data are written into and read from magnetic tape? **[5]**

Q. [8] **[a]** Differentiate between Synchronous and Asynchronous serial data transmission scheme. [5]
[b] Explain Instruction Set Architecture. (ISA). [5]

Q. [9] **[a]** Define Semiconductor memory. Explain the working of DRAM with a neat diagram. [5]
[b] Discuss instruction pipelining. [5]

Q. [10] **Write short notes on any TWO: [5+5]**
[a] Video Display unit.
[b] Gate Array.
[c] Cyclic redundancy check logic.

Downloaded from www.jayaram.com.np